In the Claims:

Please amend claim 8 and add new claims 16-18 as indicated in the following listing of claims, which replaces all previous versions.

1. (Previously presented) A driver, comprising:

a battery terminal and a ground terminal for connection to a voltage battery output and a ground battery output, respectively;

an output terminal for driving a coil;

an energise FET having a source, a gate and a drain;

a control FET having a source, a gate and drain and

a freewheel FET having a source, a gate and a drain,

wherein the energise FET is connected with source and drain between the output terminal and the ground terminal, and the control FET and freewheel FET are connected in series between the battery terminal and the output terminal, the sources and drains of the control and freewheel FETs being arranged reversely so that current flowing through the control and freewheel FETs in series flows from source to drain in one of the control and freewheel FETs and from drain to source in the other.

2. (Previously presented) A driver according to claim 1, wherein the source of the energise FET is connected to the ground terminal and the drain is connected to the output terminal;

the drain of the control FET is connected in common with the drain of the energise FET to the output terminal; and

the drain of the freewheel FET is connected to the battery terminal and the source is connected to the source of the control FET.

3. (Previously presented) A driver according to claim 1 comprising a common semiconductor substrate, wherein the drains of the control FET and the energise FET are formed in the common semiconductor substrate and the drain of the freewheel FET is isolated from the common semiconductor substrate.

4. (Previously presented) A driver according to claim 3 further comprising control circuitry integrally formed in the common semiconductor substrate, the control circuitry having a high voltage power rail connected to the battery terminal and a low voltage power rail connected to the ground terminal for powering the control circuitry from the battery and ground terminals.

5. (Previously presented) A driver according to claim 4 wherein the control circuitry includes:

high-side control circuitry integrated in the common semiconductor substrate and connected to the gates of the control and freewheel FETs to control the FETs; and

low-side control circuitry integrated in the common semiconductor substrate and connected to the gate of the energise FET to control the energise FET.

6. (Previously presented) A driver according to claim 4, wherein the control FET is arranged to have a higher gate capacitance than the freewheel FET, and the control circuitry is arranged to turn the control FET fully on in the energise mode and, on switching from the energise mode to the freewheel mode, to connect the gates of the freewheel FET and the control FET together.

7. (Previously presented) A driver according to claim 4 wherein the control circuitry further comprises temperature and voltage overload protection for protecting one or more of the energise FET, the control FET and the freewheel FET.

8. (Currently amended) A driver according to claim 4 wherein the control circuitry is arranged to switch the FETs between an energise mode in which the energise FET is on and the freewheel FET is *off*, a freewheel mode in which the energise FET is *off* and both the control and freewheel FETs are ~~off~~ on and a ring-off mode in which the energise FET is *off* and the control FET is *off*.

9. (Previously presented) A driver according to claim 3 wherein the freewheel FET is a discrete FET formed in a separate semiconductor substrate.

10. (Previously presented) A driver, comprising:

a battery terminal and a ground terminal for connection to a voltage battery output and a ground battery output, respectively;

an output terminal for driving a coil;

high and low side driver FETs integrated in a common substrate and connected between the battery terminal and the output terminal and the ground terminal and the output terminal, respectively;

high-side control circuitry capable of operation when the voltage on the common substrate is at least 1V above the voltage on the ground terminal integrated in the common semiconductor substrate, the high-side control circuitry being connected to the gates of the high side driver FET or FETs to control the high side driver FET or FETs; and

low-side control circuitry capable of operation even when the voltage on the common substrate is close to the voltage on the ground terminal integrated in the common semiconductor substrate, the low-side control circuitry being connected to the gates of the low side driver FET or FETs to control the low side driver FET or FETs.

11. (Previously presented) A driver according to any preceding claim wherein the FETs are each n-type.

12. (Previously presented) A coil control circuit, comprising:

a driver according to any preceding claim;

a battery having a voltage battery output connected to the battery terminal of the driver and a ground battery output connected to the ground terminal of the driver; and

a coil connected between the output terminal of the driver and the voltage battery output.

13. (Previously presented) A coil control circuit according to claim 12 wherein the coil is a solenoid actuator having a mechanical actuator actuated by current in the coil.

14. (Previously presented) A method of operation of a coil control circuit, comprising:

providing a coil control circuit having a coil, a battery having positive and negative outputs, and a driver, the driver having an output terminal connected through the coil to a first one of the battery outputs, an energise FET connected between the output terminal and the other one of the battery outputs; and control and freewheel FETs of the like conductivity type connected reversely in series between the output terminal and the first one of the battery output;

switching to an energise mode in which the energise FET is on and the freewheel FET is *off* to energise the coil;

switching to a freewheel mode in which the energise FET is *off* and both the control and freewheel FETs are on to retain the coil energised; and

switching to a ring-off mode in which the energise FET is *off* and the control FET is *off* to de-energise the coil.

15. (Previously presented) A method according to claim 14 further including switching the control FET fully on in the energise mode and, on switching to the freewheel mode from the energise mode, connecting the gates of the freewheel and control FETs together to share charge to switch on the freewheel FET.

16. (New) A driver according to claim 10, wherein the high side driver FETs include a control FET and a freewheel FET each having a source and a drain, the control FET and freewheel FET being connected in series between the battery terminal and the output terminal, the sources and drains of the control and freewheel FETs being arranged reversely so that current flowing through the control and freewheel FETs in series flows from source to drain in one of the control and freewheel FETs and from drain to source in the other.

17. (New) A driver according to claim 16, wherein the low side driver FET or FETs and the control FET are integrated on the common substrate, and the drain of the freewheel FET is isolated from the common substrate.

18. (New) A driver according to claim 1 incorporated into a single package with a second driver that shares the battery and ground terminals, the second driver including a second output terminal for driving a second coil, a second energise FET, a second control FET and a second freewheel FET each having respective sources, gates and drains, the second energise FET being connected with source and drain between the second output terminal and the ground terminal, and the second control FET and second freewheel FET being connected in series between the battery terminal and the second output terminal, the sources and drains of the second control and second freewheel FETs being arranged reversely so that current flowing through the second control and second freewheel FETs in series flows from source to drain in one of the second control and second freewheel FETs and from drain to source in the other.